In re Patent Application of:
CORONEL ET AL.
Serial No. **10/042,520**
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In the Claims:

Claims 1 to 10 (Previously Cancelled).

11. (Previously Added) A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the method comprising:

forming a barrier layer on a substrate, and forming a first dielectric layer on the barrier layer;

removing a portion of the first dielectric layer for defining a plurality of spaced apart openings therein;

forming a first metal layer on the first dielectric layer and in the plurality of openings;

removing the first metal layer from an upper surface of the first dielectric layer while leaving the first metal layer in the plurality of openings for forming lower electrodes of the respective storage capacitors;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a second conductive layer on the second dielectric layer and on the first dielectric layer to form a continuous upper electrode, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed;

forming a third conductive layer on the second

conductive layer;

implanting dopants in the third conductive layer corresponding to an upper portion of the zones showing the difference in topography;

removing the third conductive layer corresponding to a lower portion of the zones; and

removing the upper electrodes exposed in the lower portion of the zones, and completely removing a remainder of the third conductive layer, the removal of the upper electrodes being self-aligned with respect to the lower electrodes.

12. (Previously Added) A method according to Claim 11, further comprising forming a plurality of access transistors in the substrate.

13. (Currently Amended) A method according to Claim 11, wherein each of the ~~first,~~ first and second ~~and third~~ dielectric layers comprises silicon oxide.

14. (Previously Added) A method according to Claim 11, wherein each of the first, second and third conductive layers comprises polysilicon.

15. (Previously Added) A method according to Claim 11, wherein the DRAM comprises an embedded DRAM; and further comprising using a mask so that the dopants are only implanted in the third conductive layer corresponding to the upper portion of the zones.

16. (Previously Added) A method according to Claim 11, wherein the first conductive layer forming the lower electrodes comprises hemispherical polysilicon grains.

17. (Previously Added) A method according to Claim 11, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

18. (Previously Added) A method according to Claim 11, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

19. (Previously Added) A method according to Claim 11, wherein the dopants comprise BF_2.

20. (Previously Added) A method according to Claim 11, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the third conductive layer.

21. (Previously Added) A method according to Claim 11, wherein removing the upper electrodes and the remainder of the third conductive layer is performed by a plasma ion etching.

22. (Previously Added) A method according to Claim 21, wherein the plasma ion etching is an isotropic plasma ion etching.

23. (Previously Added) A method according to Claim 21, wherein the plasma ion etching is an anisotropic plasma ion etching.

24. (Previously Added) A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the method comprising:

forming a plurality of access transistors in a substrate;

forming a first dielectric layer on the substrate;

defining a plurality of spaced apart openings in the first dielectric layer;

forming lower electrodes for the respective storage capacitors in the plurality of spaced apart openings;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a continuous upper electrode for the respective storage capacitors on the first and second dielectric layers, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed;

forming a conductive layer on the continuous upper electrode;

implanting dopants in the conductive layer

corresponding to an upper portion of the zones showing the difference in topography;

removing the conductive layer corresponding to a lower portion of the zones; and

removing the upper electrodes exposed in the lower portion of the zones, and completely removing a remainder of the conductive layer, the removal of the upper electrodes being self-aligned with respect to the lower electrodes.

25. (Previously Added) A method according to Claim 24, wherein the DRAM comprises an embedded DRAM; and further comprising using a mask so that the dopants are only implanted in the conductive layer corresponding to the upper portion of the zones.

26. (Previously Added) A method according to Claim 24, wherein the lower electrodes comprises hemispherical polysilicon grains.

27. (Previously Added) A method according to Claim 24, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

28. (Previously Added) A method according to Claim 24, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

29. (Previously Added) A method according to Claim

24, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the conductive layer.

30. (Previously Added) A method according to Claim 24, wherein removing the upper electrodes and the remainder of the conductive layer is performed by a plasma ion etching.

31. (Previously Added) A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the method comprising:

forming a plurality of access transistors in a substrate;

forming a first dielectric layer on the substrate;

defining a plurality of spaced apart openings in the first dielectric layer;

forming lower electrodes for the respective storage capacitors in the plurality of spaced apart openings;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a continuous upper electrode for the respective storage capacitors on the first and second dielectric layers, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed; and

removing the upper electrodes exposed in a lower portion of the zones, the removal of the upper electrodes being self-aligned with respect to the lower electrodes.

Claim 32 (Cancelled).

33. (Previously Added) A method according to Claim 31, wherein the lower electrodes comprises hemispherical polysilicon grains.

34. (Previously Added) A method according to Claim 31, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

35. (Previously Added) A method according to Claim 31, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

36. (Previously Added) A method according to Claim 31, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the conductive layer.

37. (Previously Added) A method according to Claim 31, wherein removing the upper electrodes and the remainder of the conductive layer is performed by a plasma ion etching.